CLAIMS

What is claimed is:

1. A method for testing a multi-gigabit transceiver, the method comprises:

configuring the multi-gigabit transceiver for testing;

varying a performance aspect of the multi-gigabit transceiver to produce a varied multi-gigabit transceiver;

providing an input test signal to the varied multi-gigabit transceiver;

monitoring an output of the varied multi-gigabit transceiver with respect to the input test signal to determine a level of signal integrity;

determining whether the level of signal integrity provides a desired performance margin; and

when the level of signal integrity does not provide the desired performance margin, adjusting a programmable operational setting of the multi-gigabit transceiver.

2. The method of claim 1, wherein the configuring the multi-gigabit transceiver further comprises:

configuring a transmit physical media attachment module of the multi-gigabit transceiver or of another multi-gigabit transceiver to transmit the input test signal as a serial data stream; and

coupling an output of the transmit physical media attachment module to an input of a receive physical media attachment module of the multi-gigabit transceiver.

3. The method of claim 2, wherein the varying a performance aspect of the multi-gigabit transceiver further comprises at least one of:

adding jitter to a clock signal of the receive physical media attachment module or of the transmit physical media attachment module;

changing an output slew rate of the transmit physical media attachment module;

changing an amplitude of the output of the transmit physical media attachment module;

adjusting equalizer coefficients of an equalizer within the receive physical media attachment module;

adding power supply noise to a supply voltage source the transmit physical media attachment module or the receive physical media attachment module;

adding noise to the input test signal;

providing adjacent channel noise on a channel proximal to the coupling of the transmit physical media attachment module to the receive physical media attachment module; and

providing load noise on an output of the receive physical media attachment module.

4. The method of claim 3, wherein the adding the jitter to the clock signal further comprises:

adjusting a fractional divider of a phase locked loop during test mode; and

setting the fractional divider to an integer value during normal mode.

5. The method of claim 1, wherein the adjusting the programmable operational setting of the multi-gigabit transceiver further comprises at least one of:

adjusting equalization settings of an equalizer within a receive physical media attachment module of the multi-gigabit transceiver;

adjusting amplification settings of an amplifier within the receive physical media attachment module; and

adjusting a sampling point within a data detection circuit within the receive physical media attachment module.

6. The method of claim 1 further comprises:

when the level of signal integrity provides the desired performance margin, maintaining the programmable operational setting of the multi-gigabit transceiver.

7. The method of claim 1, wherein the monitoring the output of the varied multi-gigabit transceiver further comprises at least one of:

monitoring bit error rate of a receive physical media attachment module of the multi-gigabit transceiver; and

determining an eye opening of a recovered signal as produced by the receive physical media attachment module of the multi-gigabit transceiver.

8. The method of claim 1, wherein the providing the input test signal further comprises at least one of:

providing a known test pattern; and

providing a pseudo random test pattern.

9. The method of claim 1 further comprises:

providing the input test signal to the varied multi-gigabit transceiver subsequent to the step of adjusting the programmable operational setting of the multi-gigabit transceiver to produce an adjusted multi-gigabit transceiver;

monitoring an output of the adjusted multi-gigabit transceiver with respect to the input test signal to determine the level of signal integrity;

determining whether the level of signal integrity provides the desired performance margin; and

when the level of signal integrity does not provide the desired performance margin, identifying the multi-gigabit transceiver as failing test or as a reduced operational multi-gigabit transceiver.

10. A multi-gigabit transceiver comprises:

a transmit physical media attachment module operably coupled to convert parallel input data into serial output data;

a receive physical media attachment module operably coupled to convert receive serial data into receive parallel data;

a transmit physical coding sublayer module operably coupled to convert transmit data words into the parallel input data;

a receive physical coding sublayer module operably coupled to convert the receive parallel data into receive data words; and

a control module operably coupled to place the multi-gigabit transceiver in a test mode or an operation mode, wherein, when in the test mode, the control module facilitates testing of the multi-gigabit transceiver by:

configuring the multi-gigabit transceiver for testing;

varying a performance aspect of the multi-gigabit transceiver to produce a varied multi-gigabit transceiver;

providing an input test signal to the varied multi-gigabit transceiver;

monitoring an output of the varied multi-gigabit transceiver with respect to the input test signal to determine a level of signal integrity;

determining when the level of signal integrity provides a desired performance margin; and

when the level of signal integrity does not provide the desired performance margin, adjusting a programmable operational setting of the multi-gigabit transceiver.

11. The multi-gigabit transceiver of claim 10, wherein the control module further functions to configure the multi-gigabit transceiver by:

configuring the transmit physical media attachment module to transmit the input test signal as a serial data stream; and

coupling an output of the transmit physical media attachment module to an input of the receive physical media attachment module.

12. The multi-gigabit transceiver of claim 10, wherein the control module further functions to vary a performance aspect of the multi-gigabit transceiver by at least one of:

adding jitter to a clock signal of the receive physical media attachment module;

changing an output slew rate of the transmit physical media attachment module;

changing amplitude of the output of the transmit physical media attachment module;

adjusting equalizer coefficients of an equalizer within the receive physical media attachment module;

adding power supply noise to a supply voltage source the transmit physical media attachment module or the receive physical media attachment module;

adding noise to the input test signal;

providing adjacent channel noise on a channel proximal to the coupling of the transmit physical media attachment module to the receive physical media attachment module; and

providing load noise on an output of the receive physical media attachment module.

13. The multi-gigabit transceiver of claim 12, wherein the control module further functions to add the jitter to the clock signal by:

adjusting a fractional divider of a phase locked loop during test mode; and

setting the fractional divider to an integer value during normal mode.

14. The multi-gigabit transceiver of claim 10, wherein the control module further functions to adjust the programmable operational setting of the multi-gigabit transceiver by at least one of:

adjusting equalization settings of an equalizer within the receive physical media attachment module;

adjusting amplification settings of an amplifier within the receive physical media attachment module; and

adjusting a sampling point within a data detection circuit within the receive physical media attachment module.

15. The multi-gigabit transceiver of claim 10, wherein the control module further functions to:

when the level of signal integrity provides the desired performance margin, maintain the programmable operational setting of the multi-gigabit transceiver.

16. The multi-gigabit transceiver of claim 10, wherein the control module further functions to monitor the output of the varied multi-gigabit transceiver by at least one of:

monitoring bit error rate of the receive physical media attachment module; and

determining an eye opening of a recovered signal as produced by the receive physical media attachment module.

17. The multi-gigabit transceiver of claim 10, wherein the control module further functions to provide the input test signal by at least one of:

providing a known test pattern; and

providing a pseudo random test pattern.

18. The multi-gigabit transceiver of claim 10, wherein the control module further functions to:

provide the input test signal to the varied multi-gigabit transceiver subsequent to the step of adjusting the programmable operational setting of the multi-gigabit transceiver to produce an adjusted multi-gigabit transceiver;

monitor an output of the adjusted multi-gigabit transceiver with respect to the input test signal to determine the level of signal integrity;

determine whether the level of signal integrity provides the desired performance margin; and

when the level of signal integrity does not provide the desired performance margin, identify the multi-gigabit

transceiver as failing test or as a reduced operational multi-gigabit transceiver.

19. A programmable logic device comprises:

a plurality of multi-gigabit transceivers, wherein each of the multi-gigabit transceiver includes:

a transmit physical media attachment module operably coupled to convert parallel input data into serial output data;

a receive physical media attachment module operably coupled to convert receive serial data into receive parallel data;

a transmit physical coding sublayer module operably coupled to convert transmit data words into the parallel input data; and

a receive physical coding sublayer module operably coupled to convert the receive parallel data into receive data words; and

a control module operably coupled to place at least one of the plurality of multi-gigabit transceivers in a test mode or an operation mode, wherein, when in the test mode, the control module facilitates testing of the at least one of the plurality of multi-gigabit transceivers by:

configuring the at least one of the plurality of multi-gigabit transceivers for testing;

varying a performance aspect of the at least one of the plurality of multi-gigabit transceivers to produce a varied multi-gigabit transceiver;

providing an input test signal to the varied multi-gigabit transceiver;

monitoring an output of the varied multi-gigabit transceiver with respect to the input test signal to determine a level of signal integrity;

determining when the level of signal integrity provides a desired performance margin; and

when the level of signal integrity does not provide the desired performance margin, adjusting a programmable operational setting of the multi-gigabit transceiver.

20. The programmable logic device of claim 19, wherein the control module further functions to configure the at least one of the plurality of multi-gigabit transceivers by:

configuring the transmit physical media attachment module to transmit the input test signal as a serial data stream; and

coupling an output of the transmit physical media attachment module to an input of the receive physical media attachment module.

21. The programmable logic device of claim 19, wherein the control module further functions to configure the plurality of multi-gigabit transceivers for testing by:

configuring the transmit physical media attachment module of plurality of multi-gigabit transceivers to transmit the input test signal as a serial data stream; and

daisy chain coupling an output of the transmit physical media attachment module of one of the plurality of multi-gigabit transceivers to an input of the receive physical media attachment module of another one of the plurality of multi-gigabit transceivers.

22. The programmable logic device of claim 19, wherein the control module further functions to vary a performance aspect of the at least one of the plurality of multi-gigabit transceivers by at least one of:

adding jitter to a clock signal of the receive physical media attachment module;

changing an output slew rate of the transmit physical media attachment module;

changing amplitude of the output of the transmit physical media attachment module;

adjusting equalizer coefficients of an equalizer within the receive physical media attachment module;

adding power supply noise to a supply voltage source the transmit physical media attachment module or the receive physical media attachment module;

adding noise to the input test signal;

providing adjacent channel noise on a channel proximal to the coupling of the transmit physical media attachment module to the receive physical media attachment module; and

providing load noise on an output of the receive physical media attachment module.

23. The programmable logic device of claim 22, wherein the control module further functions to add the jitter to the clock signal by:

adjusting a fractional divider of a phase locked loop during test mode; and

setting the fractional divider to an integer value during normal mode.

24. The programmable logic device of claim 19, wherein the control module further functions to adjust the programmable operational setting of the at least one of the plurality of multi-gigabit transceivers by at least one of:

adjusting equalization settings of an equalizer within the receive physical media attachment module;

adjusting amplification settings of an amplifier within the receive physical media attachment module; and

adjusting a sampling point within a data detection circuit within the receive physical media attachment module.

25. The programmable logic device of claim 19, wherein the control module further functions to:

when the level of signal integrity provides the desired performance margin, maintain the programmable operational setting of the at least one of the plurality of multi-gigabit transceivers.

26. The programmable logic device of claim 19, wherein the control module further functions to monitor the output of the varied multi-gigabit transceiver by at least one of:

monitoring bit error rate of the receive physical media attachment module; and

determining an eye opening of a recovered signal as produced by the receive physical media attachment module.

27. The programmable logic device of claim 19, wherein the control module further functions to provide the input test signal by at least one of:

providing a known test pattern; and

providing a pseudo random test pattern.

28. The programmable logic device of claim 19, wherein the control module further functions to:

provide the input test signal to the varied multi-gigabit transceiver subsequent to the step of adjusting the programmable operational setting of the multi-gigabit transceiver to produce an adjusted multi-gigabit transceiver;

monitor an output of the adjusted multi-gigabit transceiver with respect to the input test signal to determine the level of signal integrity;

determine whether the level of signal integrity provides the desired performance margin; and

when the level of signal integrity does not provide the desired performance margin, identify the multi-gigabit transceiver as failing test or as a reduced operational multi-gigabit transceiver.